AMMENDMENTS TO THE DRAWINGS

Please replace Figure 1 with the attached Figure 1 Replacement Sheet.

REMARKS

Mischaracterization of Cited References

Applicant respectfully contends that the Office Action mischaracterizes the cited references. In particular, the Office Action asserts that Zitlaw et al. and McClain both teach systems having a processor coupled to volatile and non-volatile memory devices that, as a whole, present themselves as a synchronous memory device through an external synchronous memory interface and therefore function as a unitary synchronous memory device. In addition, the Office Action asserts that the "memory device" systems of Zitlaw et al. and McClain buffer reads and writes to their coupled non-volatile memory devices in their volatile memory devices. *See, e.g.,* Final Office Action mailed on February 5, 2007, pages 5, 9-10 and 16-18.

While Applicant acknowledges that Zitlaw et al. and McClain do indeed have controllers or processors coupled to both volatile and non-volatile memory devices, the references only purport to present conventional computer systems, and do not disclose that the systems have an external synchronous memory interface or that the systems present themselves externally as a memory device through this external synchronous memory interface. *See, e.g.,* Zitlaw et al., Abstract, Figures 1A and 1B, Paragraphs [0008]-[0009] and [0036]-[0037]; McClain, Figures 1 and 2, Abstract, and Column 3, Line 20 to Column 5, Line 6. Thus, the systems of Zitlaw et al. and McClain, while having both volatile and non-volatile memory devices, cannot be used themselves in larger systems as unitary synchronous memory device components having an external synchronous memory device interface. Therefore, there is no teaching in the references, either expressly or inherently, that the systems of Zitlaw et al. and McClain are capable of presenting themselves externally through an external synchronous memory interface as a unitary synchronous memory device. The Examiner further provides no support or reasoned statement as to how the systems of Zitlaw et al. and McClain are capable of presenting themselves externally through an external synchronous memory interface as a unitary synchronous memory device based on the Zitlaw et al. and McClain references. In addition, contrary to the Examiner's assertion, the cited references teach away from this in disclosing that the processors themselves are the end users of the coupled volatile and non-volatile memory devices of the systems, stating that they hold the BIOS or boot code for the systems (as contrasted to them

storing code and data for an external system they are an integral part of). *See, e.g.,* Zitlaw et al., Paragraph [0004] ("Many modern personal computers (PCs) and processor based systems have their basic input/output system (BIOS) code stored on a Flash memory chip so that it can easily be updated if necessary. Such a BIOS is sometimes called a Flash BIOS. In a PC or processor based system, the memory that stores the BIOS code is typically called the "boot memory", as it is usually the first code that the processor executes upon reset or power up. The code the boot memory contains initializes the system, sets up basic environmental variables and interrupt vectors, initializes peripherals, and, finally, loads and begins execution of the operating system (OS) or main executable of the PC or processor based system."); McClain, Column 3, Lines 53-55 ("The system processor 14 starts the system initialization process by issuing reads to the non-volatile memory address range..")

In contrast, Applicant has taught and claimed devices to facilitate use of a controller, an external synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a unitary synchronous memory device that can be used as a direct replacement for volatile synchronous memory devices. *See, e.g.,* Specification, the memory devices 100, 204, 304 of Figures 1, 2, and 3A-3B; paragraph 0023 ("..High density non-volatile memory subsystems and devices of the present invention incorporate a synchronous interface to allow them to be utilized as a conventional memory device. Memory device embodiments of the present invention utilize an external or embedded controller and/or memory buffer to present the high density non-volatile memory device(s) as a conventional memory device having a synchronous interface. This allows the high density non-volatile memory embodiments of the present invention to support in-place code execution and allow them to be booted from. Additionally, the memory buffer allows for caching/buffering of data read and/or write accesses, allowing high density non-volatile memory devices of the present invention to be quickly accessed as if they were conventional synchronous RAM memory devices. In one embodiment of the present invention, a high density non-volatile memory device eliminates the requirement of external drivers, a memory controller, a

customized interface port on a microprocessor, and/or operating system support to utilize a specialized high density non-volatile memory device, and in particular, a NAND architecture Flash memory device. This simplifies the use and design effort of high density non-volatile memories by reducing specialized interfacing, while reducing the overall production cost through allowing use of a less expensive NAND architecture Flash memory or other high density non-volatile memory where a more expensive memory device would normally be required.."). Such features are variously claimed by Applicant in the pending claims.

Because the various rejections each rely on the erroneous characterization of the cited references, Applicant contends that the Office has not made a *prima facie* case of anticipation or obviousness against Applicant's pending claims. Accordingly, and as further detailed below, Applicant contends that the pending claims are patentably distinct from the cited references.

Amendments to the Drawings

The Examiner stated that the drawings were objected to under 37 C.F.R. §1.83(a). The Examiner stated that the drawings do not show every feature of the invention specified in the claims, stating that "the external 'ready/busy' pin and the status register must be shown or the feature(s) canceled from the claim(s)." Applicant respectfully disagrees with the Examiner and believes that no modifications to the drawings are required under 37 CFR 1.83(a), contending that these features are clearly shown and described in, at least, Figures 1, 2, and 3A-3B, which detail systems incorporating non-volatile memory devices having control lines 106, 208, 308, control registers 114 and controller 212, 312, and also in the Specification in at least Paragraphs [0030], [0034], and [0038]-[0041] of the Application.

However, in the interest of furthering prosecution of the Present Application, Applicant has amended Figure 1 herein to add the status register 132 and ready/busy pin 134, as required by the Examiner. A Replacement Sheet is attached to this Office Action Response. Applicant submits that this amendment is supported by the Specification and introduces no new matter thereby. Paragraph [0033] has also been appropriately amended to address the amendment to Figure 1.

As such, Applicant submits that the requirements of MPEP §608.02, §608.02(d) and 37 CFR 1.83(a) that "[t]he drawing in a nonprovisional application must show every feature of the invention specified in the claims" are met and that one skilled in the art would recognize the external "ready/busy" pin and the status register as having been disclosed and enabled. The Applicant therefore requests the objection to the drawings by the Examiner under 37 CFR 1.83(a) be withdrawn and that the formal drawings be approved.

In the Specification

As stated above, Applicant notes that Paragraph [0033] of the Specification has been amended herein to support the amendment of Figure 1 and reference the call outs of the optional elements, status register 132 and ready/busy pin 134. Applicant submits that this amendment is supported by the Specification and introduces no new matter thereby.

The Examiner also objected to the specification and stated it failed to provide proper antecedent basis for the claimed subject matter. The Examiner stated that "[t]he clear support and antecedent basis is not found for the term 'an external synchronous memory interface' in the specification of the current application in such a way so that the meaning of the terms in the claims may be ascertainable by the reference to the description." (*See,* Final Office Action mailed on February 5, 2007, Page 3, Item 4.)

Applicant respectfully disagrees and contends that the external synchronous memory interface of embodiments of the present invention are detailed in at least Paragraphs [0007]-[0009], [0011]-[0017], [0023], [0030]-[0032], [0035], [0038], [0040]-[0042] and [0044]-[0046] and Figures 1-3B of the Present Application.

In particular, Applicant notes Paragraph [0011] which states, in part, "[a]lthough described in relation to NAND architecture Flash memory, the various embodiments relate generally to non-volatile memory devices and subsystems that incorporate a synchronous interface. Memory device embodiments of the present invention utilize an external or embedded controller and/or memory buffer to present the non-volatile memory device(s) as a conventional memory device having a synchronous interface." Paragraph [0030], which states, in part, "[t]he

NAND architecture Flash memory device 100 has a synchronous interface 130 that contains an address interface 104, control interface 106, and data interface 108 that are each coupled to the processing device 102 to allow synchronous memory read and write accesses." And Paragraph [0044], which states "It is also noted that other architectures of high density non-volatile memory systems, external synchronous interfaces, and manners of coupling the memory controller to the high density non-volatile memory devices, such as directly coupled individual control busses and signal lines, are possible and should be apparent to those skilled in the art with benefit of the present disclosure. It is also noted that other formats and pairings of high density non-volatile memory devices or other non-volatile memory devices in a memory subsystem or memory device are possible and should be apparent to those skilled in the art with benefit of the present disclosure." Applicant further respectfully notes that the Present Application is titled "NON-VOLATILE MEMORY WITH SYNCHRONOUS DRAM INTERFACE."

As such, Applicant submits that the requirements of MPEP §608.01(o) and 37 CFR 1.75(d)(1) are met and that one skilled in the art would recognize an external synchronous memory interface as having been disclosed and enabled. The Applicant therefore requests the objection to the specification by the Examiner under MPEP §608.01(o) and 37 CFR 1.75(d)(1) be withdrawn and the specification be approved.

Claim Rejections Under 35 U.S.C. § 112

Claims 1-99 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully traverses this rejection and feels that claims 1-99 are allowable for the following reasons.

As stated above, Applicant respectfully disagrees and contends that the external synchronous memory interface of embodiments of the present invention are detailed in at least Paragraphs [0007]-[0009], [0011]-[0017], [0023], [0030]-[0032], [0035], [0038], [0040]-[0042] and [0044]-[0046] and Figures 1-3B of the Present Application.

Specifically, Applicant contends that the Specification of the Present Application discloses and enables a non-volatile memory device(s) as being adapted to present an external

synchronous memory interface and, in particular, present and act as a volatile memory type through the synchronous interface.

As such, the Applicant therefore respectfully requests that the rejection of claims 1-99 under 35 U.S.C. § 112, second paragraph be withdrawn as claims 1-99, clearly define and enable one of ordinary skill in the art to make and use the claimed invention .

Claim Rejections Under 35 U.S.C. § 102

Claims 1, 10-13, 17-22, 27-28, 34-35, 39-46, 52, 54-61, 67-68, 70-75, 79-80, 86-87 and 89-99 were rejected under 35 U.S.C. § 102(e) as being anticipated by Zitlaw et al. (U.S. Patent Publication No. 2004-0128425). Applicant respectfully traverses this rejection and requests reconsideration of the claims. Applicant reserves the right to swear behind the reference Zitlaw, but feels that claims 1, 10-13, 17-22, 27-28, 34-35, 39-46, 52, 54-61, 67-68, 70-75, 79-80, 86-87 and 89-99 are allowable for the following reasons. Applicant continues to respectfully disagree and maintains that the Examiner is mischaracterizing the reference in maintaining that the system 150 of Zitlaw et al. is a memory device.

On page 16 of the Final Office Action mailed February 5, 2007, the Examiner stated in his response to Applicant's remarks that "[w]ith respect to (a), Examiner would like to point out to Applicant that the controller (i.e. 152 in Fig. 1 B) of Zitlaw et al. prior art does present the non-volatile memory device (i.e. 150 in Fig. 1 B) as a synchronous memory device (i.e. since each memory (1 56, 158 and 160 in Fig. 1 B) of the non-volatile memory array can be synchronous memories, the memory device (150) as a whole functions a synchronous memory device) through the synchronous memory interface (i.e. 154 in Fig. 1 B), as claimed in the current application (e.g. see Fig. 1 B and paragraph [0036])."

Applicant respectfully continues to maintain, as stated above in "Mischaracterization of the Cited References", that Zitlaw et al. discloses a system 150 and not a memory device, as maintained by the Examiner. Applicant further maintains that this would be understood as such by one of ordinary skill in the art.

Applicant submits that embodiments of the Present Application (the memory devices 100, 204, 304 of Figures 1, 2, and 3A-3B of the Present Application) would interface into the system 150 of Zitlaw et al. by coupling to the memory bus 154 as one of the memory devices 156, 158, 160. As such, Applicant contends that the memory device embodiments of the Present Application would not be the system 150 of Zitlaw et al., as the Examiner asserts, but a memory device 156, 158, 160 to insert into it.

Specifically, Applicant maintains that the system 150 of Zitlaw et al. is not disclosed as a memory device 156, 158, 160, but as a system 150. Applicant also maintains that Zitlaw et al. does not teach or disclose that the system 150 presents itself, and the memory devices 156, 158, 160 coupled to it on the internal SDRAM memory bus 154, through a separate external SDRAM interface on the controller 152 as being a unitary SDRAM device in its own right or as emulating a unitary SDRAM DRAM. Applicant further maintains that Paragraph [0036] of Zitlaw et al., cited by the Examiner, only discloses that the SDRAM memory bus 154 is an SDRAM interface bus internal to the system and has the synchronous memory devices 156, 158, 160 coupled to it; stating "[0036] FIG. 1B shows a system 150 embodiment of the present invention. In FIG. 1B, the system 150 includes a memory controller 152, a SDRAM interface memory bus 154 containing address, data, and control lines, and one or more synchronous memories (SDRAM or DDR-SDRAM) 156, 158, 160. Each SDRAM memory device 156, 158, 160 on the SDRAM interface memory bus 154 is coupled to a chip select line 162, 164, 166. The chip select lines 162, 164, 166 of the one or more synchronous memories (SDRAM or DDR-SDRAM) 156,158, 160 are typically position dependent in the system 150 of FIG. 1B. For example, memory 0 156 is coupled to chip select 0 (CS0) 162, memory 1 158 is coupled to chip select 1 (CS1) 162, the memory 2 160 is coupled to chip select 2 (CS0) 166, and so forth." In addition, Applicant contends that one of ordinary skill in the art would not recognize Zitlaw et al. as disclosing a memory device 156, 158, 160 presenting an external synchronous interface to the outside world, but as a memory system 150 with a processor/controller 152 incorporating an internal SDRAM bus 154 and memory devices 156, 158, 160.

Also on page 17 the Final Office Action mailed February 5, 2007, the Examiner stated in his response to Applicant's remarks regarding Zitlaw et al. disclosing shadow memory or that the

volatile memory of Zitlaw et al. is used as buffer memory that "[w]ith respect to (b), Examiner maintains that the Zitlaw et al. prior art clearly discloses that the decoder maps the individual memory device or portion of an individual memory device address range into the physical address range of the memory subsystem (e.g. see paragraph [0008]) and since the one or more memory devices (i.e. 156, 158, and 160 in Fig. 1B) are synchronous memory devices, it operates as shadow memory, i.e. by eliminating the need for separate shadow RAM in the system. Furthermore, the memory 156 in Fig. 1B of the Zitlaw et al. prior art is SDRAM memory and SDRAM memory is a 'fast' volatile memory, i.e. it can be used as read and/or write data buffer memory, "scratch pad" memory, or temporary or cache memory as claimed in this application (e.g. see paragraphs [0006] and [0008] and Fig. 1B)."

Applicant respectfully continues to disagree and maintains, as stated above, that Zitlaw et al. does not disclose a memory device 156, 158, 160, but as a system 150. In addition, as stated before, Applicant has carefully reviewed Zitlaw et al. and, in particular, Paragraphs [0008], [0036]-[0039] and Figure 1B of Zitlaw et al., and can find no mention of the controller remapping addresses of one or more DRAM memory array sections in the system 150 of Figure 1B to the synchronous memory interface to operate as "shadow" memory, or the utilization of the DRAM as an extended read and/or write data buffer memory, "scratch pad" memory, or temporary or cache memory. In particular, Applicant maintains that the system 150 of Figure 1B does not disclose a shadow ram, as it does not need it; as disclosed in Zitlaw et al. the SyncFlash memory 158 is a non-volatile memory that can be read as fast as a volatile SDRAM memory and interfaces to the SDRAM memory bus, thus eliminating the need for shadow ram in the system 150 of Figure 1B. In addition, while the other SDRAM memory devices 156 and 160 of Figure 1B of Zitlaw et al. may be volatile, Zitlaw et al. does not disclose the system 150 of Figure 1B as utilizing them as a buffer memory, "scratch pad" memory, temporary or cache memory, or the controller being adapted to use the SDRAM 156, 160 as such. Applicant therefore respectfully maintains that Zitlaw et al. does not disclose using the DRAM memory devices as a buffer memory "shadow" memory, "scratch pad" memory, temporary or cache memory, or the controller being adapted to use the SDRAM as such. If, alternatively, the Examiner is arguing that such use of the volatile SDRAM in Zitlaw et al. is inherent or is taking Official Notice of

such, Applicant herein continues to traverse any such assertion and requests a reasoned argument or secondary reference to support any such position by the Examiner. Applicant respectfully submits that if the Examiner maintains that this is an inherent feature, the Examiner has the burden of proving that the inherent element must of necessity only work in the manner of the Applicant's claimed invention. If any other interpretation is possible for the inherent element relied upon for the rejection, the rejection cannot be maintained.

Applicant therefore respectfully continues to maintain that in Figure 1B, Zitlaw et al. only discloses a system 150 having processor or controller 152 with a SDRAM memory bus 154, wherein the SDRAM memory bus 154 has a SyncFlash memory device 158 and several SDRAM DRAM memory devices 156, 160 coupled to it. As disclosed in Paragraphs [0008]-[0009] and [0036]-[0037], the system 150 is a computer or memory subsystem itself that has an internal SDRAM memory bus 154 used to access the coupled memory devices 156, 158, 160. Zitlaw et al. does not teach or disclose that the system 150 presents itself, and the coupled memory devices 156, 158, 160, through an external SDRAM interface as being a SDRAM device in its own right or as emulating a SDRAM DRAM. Applicant therefore respectfully submits that Zitlaw et al. does not teach or disclose a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See, e.g.*, Zitlaw et al., Abstract; Figures 1A and 1B; Paragraphs [0008]-[0009] and [0036]-[0037].

In addition, as disclosed in Paragraph [0006] of Zitlaw et al., the SyncFlash memory device 158 is a Flash memory device that itself has a SDRAM compatible interface and control circuitry to allow itself to be utilized in a SDRAM memory bus; the controller 152 does not have to provide and manage an SDRAM interface for it, it already has one. *See, e.g.*, Zitlaw et al., Figure 1B and Paragraph [0006].

The Examiner also stated that "[w]ith respect to (c), the Zitlaw et al. prior art teaches the memory device (i.e. 150 in Fig. 1B) having memory arrays (i.e. 158 and 160 in Fig. 1 B) and a controller (i.e. 152 in Fig. 1B) as claimed and shown in Figs. 2, 3A and 3B of the current application."

Applicant again notes, as stated above, that the Examiner is mischaracterizing the cited references and seems to interchangeably use memory array and memory device, or system and memory device. Applicant notes that the elements of the external address interface and presentation as a unitary synchronous memory device are missing from the reference Zitlaw et al. and are required by the Applicant's claims. Applicant also respectfully maintains that one skilled in the art would recognize systems, memory devices and memory arrays as not being interchangeable.

The Examiner also stated that "[w]ith respect to (d), the Zitlaw et al. prior art does teach about remapping addresses of one or more DRAM memory array sections to the synchronous memory interface to operate as "shadow" memory by mapping the individual memory device or portion of an individual memory device address range into the physical address range of the memory subsystem. Chip select lines can also be used to map memory devices into the physical address range of the memory subsystem by selectively activating one or more individual memory devices for access as part of the address range of the memory subsystem in isolation from other addressable on the same memory interface bus (e.g. see paragraph [0008])." (Final Office Action mailed February 5, 2007, Pages 17-18).

Applicant has carefully reviewed Zitlaw et al. and, in particular, Paragraph [0008] of Zitlaw et al., and can find no mention of the controller remapping addresses of one or more DRAM memory array sections to the synchronous memory interface to operate as "shadow" memory (copying the code contents of slower non-volatile memory into faster access DRAM for execution and use), only virtual memory operation and the decoding of memory devices utilizing chip selects and address ranges. In addition, Application can find no mention of the utilization of the DRAM, explicitly or inherently, as an extended read and/or write data buffer memory,

"scratch pad" memory, or temporary or cache memory. Applicant therefore respectfully maintains that Zitlaw et al. does not disclose using the DRAM memory devices as a buffer memory "shadow" memory, scratch pad" memory, temporary or cache memory, or the controller being adapted to use the SDRAM as such.

Applicant therefore respectfully submits that Zitlaw et al. does not teach or disclose a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. Applicant thus respectfully submits that Zitlaw et al. does not teach or disclose all elements of the Applicant's claimed invention.

Applicant's claim 1, recites, "[a] non-volatile memory device comprising: a non-volatile memory array; a buffer memory; an external synchronous memory interface; and a controller coupled to the non-volatile memory array, the buffer memory, and the external synchronous memory interface, wherein the controller is adapted to interface to and manage the non-volatile memory array and buffer memory and to present the non-volatile memory device as a synchronous memory device through the external synchronous memory interface." As detailed above, Applicant submits that Zitlaw et al. fails to teach or disclose such a non-volatile memory device having a controller, a non-volatile memory array, a buffer memory, and an external synchronous memory interface, wherein the controller is adapted to manage and present the non-volatile memory array and buffer memory through the external synchronous interface as a synchronous memory device. As such, Zitlaw et al. fails to teach or disclose all elements of independent claim 1.

Applicant's claim 22, recites, "[a] NAND architecture Flash memory device comprising: a NAND architecture Flash memory array; a buffer memory; an external synchronous memory interface; and a controller coupled to the NAND architecture Flash memory array, the buffer memory, and the external synchronous memory interface, wherein the controller is adapted to interface to and manage the NAND architecture Flash memory array and to portray the NAND architecture Flash memory device as a synchronous memory device through the external

synchronous memory interface." As detailed above, Applicant submits that Zitlaw et al. fails to teach or disclose such a NAND architecture Flash memory device having a controller, a NAND architecture Flash memory array, a buffer memory, and an external synchronous memory interface, wherein the controller is adapted to manage and present the NAND architecture Flash memory array and buffer memory through the external synchronous interface as a synchronous memory device. As such, Zitlaw et al. fails to teach or disclose all elements of independent claim 22.

Applicant's claim 27, recites, "[a] non-volatile memory subsystem comprising: one or more non-volatile memory devices; a buffer memory; an external synchronous memory interface; and a controller coupled to the one or more non-volatile memory devices, the buffer memory, and the external synchronous memory interface, wherein the controller is adapted to interface to and manage the non-volatile memory devices and to present the non-volatile memory devices as a synchronous memory device through the external synchronous memory interface." As detailed above, Applicant submits that Zitlaw et al. fails to teach or disclose such a non-volatile memory subsystem having a controller, one or more non-volatile memory devices, a buffer memory, and an external synchronous memory interface, wherein the controller is adapted to manage and present the one or more non-volatile memory devices and buffer memory through the external synchronous interface as a synchronous memory device. As such, Zitlaw et al. fails to teach or disclose all elements of independent claim 27.

Applicant's claim 45, recites, "[a] system comprising: a host; and one or more non-volatile memory devices coupled to the host, wherein each of the one or more non-volatile memory devices comprises, a non-volatile memory array; a buffer memory; an external synchronous memory interface; and a controller coupled to the non-volatile memory array, the buffer memory, and the external synchronous memory interface, wherein the controller is adapted to interface to and manage the non-volatile memory array and to present the non-volatile memory device as a synchronous memory device through the external synchronous memory interface." As detailed above, Applicant submits that Zitlaw et al. fails to teach or disclose such a system. As such, Zitlaw et al. fails to teach or disclose all elements of independent claim 45.

Applicant's claim 60, recites, "[a] method of operating a non-volatile memory device comprising: managing the non-volatile memory device with an internal controller; presenting the non-volatile memory device as a synchronous memory device through an external synchronous memory interface; and buffering data access requests received through the external synchronous memory interface in an internal buffer memory." As detailed above, Applicant submits that Zitlaw et al. fails to teach or disclose such a method of operating a non-volatile memory device. As such, Zitlaw et al. fails to teach or disclose all elements of independent claim 60.

Applicant's claim 75, recites, "[a] method of operating a NAND architecture Flash memory device comprising: managing the NAND architecture Flash memory device with an internal controller; presenting the NAND architecture Flash memory device as a synchronous memory device through an external synchronous memory interface; and buffering data access requests received through the external synchronous memory interface in an internal buffer memory." As detailed above, Applicant submits that Zitlaw et al. fails to teach or disclose such a method of operating a NAND architecture Flash memory device. As such, Zitlaw et al. fails to teach or disclose all elements of independent claim 75.

Applicant's claim 94, recites, "[a] machine-usable medium, the machine-usable medium containing a software routine for causing a memory controller to execute a method, wherein the method comprises: managing one or more non-volatile memory devices with the memory controller; presenting one or more non-volatile memory devices as a synchronous memory device through an external synchronous memory interface; and buffering data access requests received through the external synchronous memory interface in a buffer memory." As detailed above, Applicant submits that Zitlaw et al. fails to teach or disclose such a machine-usable medium and method. As such, Zitlaw et al. fails to teach or disclose all elements of independent claim 94.

Applicant's claim 96, recites, "[a] system comprising: a host; and one or more non-volatile memory devices coupled to the host, wherein each of the one or more non-volatile memory devices comprises, a non-volatile memory array; a buffer memory; and an external synchronous memory interface, wherein the non-volatile memory devices comprises a means for interfacing with, managing, and buffering data access to the non-volatile memory array and

comprises a means for presenting the non-volatile memory device as a synchronous memory device through the external synchronous memory interface." As detailed above, Applicant submits that Zitlaw et al. fails to teach or disclose such a system. As such, Zitlaw et al. fails to teach or disclose all elements of independent claim 96.

Applicant's claim 98, recites, "[a] NAND architecture Flash memory subsystem comprising: one or more NAND architecture Flash memory devices; a buffer memory; an external synchronous memory interface; and a controller coupled to the one or more NAND architecture Flash memory devices, the buffer memory, and the external synchronous memory interface, wherein the controller is adapted to interface to and manage the NAND architecture Flash memory devices and to present the NAND architecture Flash memory devices as a synchronous memory device through the external synchronous memory interface." As detailed above, Applicant submits that Zitlaw et al. fails to teach or disclose such a NAND architecture Flash memory subsystem. As such, Zitlaw et al. fails to teach or disclose all elements of independent claim 98.

Applicant's claim 99, recites, "[a] method of operating a NAND architecture Flash memory subsystem comprising: managing one or more NAND architecture Flash memory devices with a controller; presenting the one or more NAND architecture Flash memory devices as a synchronous memory device through an external synchronous memory interface; and buffering data access requests received through the external synchronous memory interface in a buffer memory." As detailed above, Applicant submits that Zitlaw et al. fails to teach or disclose such a method. As such, Zitlaw et al. fails to teach or disclose all elements of independent claim 99.

Applicant respectfully contends that claims 1, 22, 27, 45, 60, 75, 94, 96, and 98-99 as pending have been shown to be patentably distinct from the cited reference of Zitlaw et al. As claims 10-13, 17-21, 28, 34-35, 39-44, 46, 52, 54-59, 61, 67-68, 70-74, 79-80, 86-87, 89-93, and 97 depend from and further define claims 1, 17, 29, 40, 48 and 96, respectively, they are also believed to be allowable. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(e) and allowance of claims 1, 10-13, 17-22, 27-28, 34-35, 39-46, 52, 54-61, 67-68, 70-75, 79-80, 86-87 and 89-99.

Claims 1, 22, 27, 45, 60, 75, 79, 94, 96 and 98-99 were rejected under 35 U.S.C. § 102(e) as being anticipated by McClain (U.S. Patent No. 7,058,779). Applicant respectfully traverses this rejection and requests reconsideration of the claims. Applicant reserves the right to swear behind the reference McClain, but feels that claims 1, 22, 27, 45, 60, 75, 79, 94, 96 and 98-99 are allowable for the following reasons.

Applicant respectfully continues to maintain, as stated above, that the Examiner is mischaracterizing the reference, and contends that McClain discloses a personal computer system 10 having a system control logic ASIC 68 coupled to several memory devices 16, 18, 20, and not a memory device itself, as maintained by the Examiner.

The Examiner stated the Final Office Action mailed February 5, 2007, Page 18, that "[w]ith respect to (e), similar to the current claimed invention, McClain does teach a memory device (i.e. 10 in Fig. 1) having a non-volatile memory array (i.e. 20 in Fig. 1); a buffer memory (i.e. 16 in Fig. 1); a synchronous memory interface (i.e. the SDRAM interface logic); and a controller (i.e. SDRAM memory controller in Fig. 2). Examiner also would like to point out to Applicant that even though, similar to the McClain prior art, the component 204 in the Fig. 2 has a memory array (224), memory controller (212), the buffer memory (218), and the memory interface (232), it is called a memory device instead of a system."

Applicant again notes, as stated above, that the Examiner is mischaracterizing the cited references and seems to interchangeably use memory array and memory device, or system and memory device. Applicant notes that the elements of the external address interface and presentation as a unitary synchronous memory device are missing from the reference McClain and are required by the Applicant's claims. Applicant also respectfully maintains that one skilled in the art would recognize systems, memory devices and memory arrays as not being interchangeable.

Applicant maintains that embodiments of the Present Application (the memory devices 100, 204, 304 of Figures 1, 2, and 3A-3B of the Present Application) would interface into the system control logic ASIC 68 of McClain by coupling to the memory bus as one of the memory devices 16, 18, 20. As such, Applicant contends that the memory device embodiments of the

Present Application would not be the system 10 or system control logic ASIC 68 and coupled memory devices 16, 18, 20 of McClain, as the Examiner asserts, but a memory device 16, 18, 20 to insert into it.

Specifically, Applicant maintains that the system 10 and/or system control logic ASIC 68 and coupled memory devices 16, 18, 20 of McClain is not disclosed as a memory device 16, 18, 20, but as a system 10 having a CPU 14 coupled to a system control logic ASIC 68, where the system control logic ASIC 68 is coupled to several memory devices 16, 18, 20. Applicant also maintains that McClain does not teach or disclose that the system control logic ASIC 68 of the system 10 presents itself, and the memory devices 16, 18, 20 coupled to it through a separate external SDRAM interface on the controller 152 as being a SDRAM device in its own right or as emulating a SDRAM DRAM. In addition, Applicant contends that one of ordinary skill in the art would not recognize McClain as disclosing a memory device 16, 18, 20 presenting an external synchronous SDRAM interface to the outside world, but as a computer system 10 with a the system control logic ASIC/memory controller 68 coupled to SDRAM memory devices 18 and 20 on an internal SDRAM bus. *See*, McClain, Figures 1 and 2; Abstract; and Column 3, Line 20 to Column 5, Line 6.

Applicant therefore respectfully submits that McClain does not teach or disclose a synchronous memory device or memory subsystem that has a controller, an external synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. Applicant thus respectfully submits that McClain does not teach or disclose all elements of the Applicant's claimed invention.

Applicant's claim 1, recites, "[a] non-volatile memory device comprising: a non-volatile memory array; a buffer memory; an external synchronous memory interface; and a controller coupled to the non-volatile memory array, the buffer memory, and the external synchronous memory interface, wherein the controller is adapted to interface to and manage the non-volatile memory array and buffer memory and to present the non-volatile memory device as a synchronous memory device through the external synchronous memory interface." As detailed

above, Applicant submits that McClain fails to teach or disclose such a non-volatile memory device having a controller, a non-volatile memory array, a buffer memory, and an external synchronous memory interface, wherein the controller is adapted to manage and present the non-volatile memory array and buffer memory through the external synchronous interface as a synchronous memory device. As such, McClain fails to teach or disclose all elements of independent claim 1.

Applicant's claim 22, recites, "[a] NAND architecture Flash memory device comprising: a NAND architecture Flash memory array; a buffer memory; an external synchronous memory interface; and a controller coupled to the NAND architecture Flash memory array, the buffer memory, and the external synchronous memory interface, wherein the controller is adapted to interface to and manage the NAND architecture Flash memory array and to portray the NAND architecture Flash memory device as a synchronous memory device through the external synchronous memory interface." As detailed above, Applicant submits that McClain fails to teach or disclose such a NAND architecture Flash memory device having a controller, a NAND architecture Flash memory array, a buffer memory, and an external synchronous memory interface, wherein the controller is adapted to manage and present the NAND architecture Flash memory array and buffer memory through the external synchronous interface as a synchronous memory device. As such, McClain fails to teach or disclose all elements of independent claim 22.

Applicant's claim 27, recites, "[a] non-volatile memory subsystem comprising: one or more non-volatile memory devices; a buffer memory; an external synchronous memory interface; and a controller coupled to the one or more non-volatile memory devices, the buffer memory, and the external synchronous memory interface, wherein the controller is adapted to interface to and manage the non-volatile memory devices and to present the non-volatile memory devices as a synchronous memory device through the external synchronous memory interface." As detailed above, Applicant submits that McClain fails to teach or disclose such a non-volatile memory subsystem having a controller, one or more non-volatile memory devices, a buffer memory, and an external synchronous memory interface, wherein the controller is adapted to manage and present the one or more non-volatile memory devices and buffer memory through

the external synchronous interface as a synchronous memory device. As such, McClain fails to teach or disclose all elements of independent claim 27.

Applicant's claim 45, recites, "[a] system comprising: a host; and one or more non-volatile memory devices coupled to the host, wherein each of the one or more non-volatile memory devices comprises, a non-volatile memory array; a buffer memory; an external synchronous memory interface; and a controller coupled to the non-volatile memory array, the buffer memory, and the external synchronous memory interface, wherein the controller is adapted to interface to and manage the non-volatile memory array and to present the non-volatile memory device as a synchronous memory device through the external synchronous memory interface." As detailed above, Applicant submits that McClain fails to teach or disclose such a system. As such, McClain fails to teach or disclose all elements of independent claim 45.

Applicant's claim 60, recites, "[a] method of operating a non-volatile memory device comprising: managing the non-volatile memory device with an internal controller; presenting the non-volatile memory device as a synchronous memory device through an external synchronous memory interface; and buffering data access requests received through the external synchronous memory interface in an internal buffer memory." As detailed above, Applicant submits that McClain fails to teach or disclose such a method of operating a non-volatile memory device. As such, McClain fails to teach or disclose all elements of independent claim 60.

Applicant's claim 75, recites, "[a] method of operating a NAND architecture Flash memory device comprising: managing the NAND architecture Flash memory device with an internal controller; presenting the NAND architecture Flash memory device as a synchronous memory device through an external synchronous memory interface; and buffering data access requests received through the external synchronous memory interface in an internal buffer memory." As detailed above, Applicant submits that McClain fails to teach or disclose such a method of operating a NAND architecture Flash memory device. As such, McClain fails to teach or disclose all elements of independent claim 75.

Applicant's claim 94, recites, "[a] machine-usable medium, the machine-usable medium containing a software routine for causing a memory controller to execute a method, wherein the method comprises: managing one or more non-volatile memory devices with the memory

controller; presenting one or more non-volatile memory devices as a synchronous memory device through an external synchronous memory interface; and buffering data access requests received through the external synchronous memory interface in a buffer memory." As detailed above, Applicant submits that McClain fails to teach or disclose such a machine-usable medium and method. As such, McClain fails to teach or disclose all elements of independent claim 94.

Applicant's claim 96, recites, "[a] system comprising: a host; and one or more non-volatile memory devices coupled to the host, wherein each of the one or more non-volatile memory devices comprises, a non-volatile memory array; a buffer memory; and an external synchronous memory interface, wherein the non-volatile memory devices comprises a means for interfacing with, managing, and buffering data access to the non-volatile memory array and comprises a means for presenting the non-volatile memory device as a synchronous memory device through the external synchronous memory interface." As detailed above, Applicant submits that McClain fails to teach or disclose such a system. As such, McClain fails to teach or disclose all elements of independent claim 96.

Applicant's claim 98, recites, "[a] NAND architecture Flash memory subsystem comprising: one or more NAND architecture Flash memory devices; a buffer memory; an external synchronous memory interface; and a controller coupled to the one or more NAND architecture Flash memory devices, the buffer memory, and the external synchronous memory interface, wherein the controller is adapted to interface to and manage the NAND architecture Flash memory devices and to present the NAND architecture Flash memory devices as a synchronous memory device through the external synchronous memory interface." As detailed above, Applicant submits that McClain fails to teach or disclose such a NAND architecture Flash memory subsystem. As such, McClain fails to teach or disclose all elements of independent claim 98.

Applicant's claim 99, recites, "[a] method of operating a NAND architecture Flash memory subsystem comprising: managing one or more NAND architecture Flash memory devices with a controller; presenting the one or more NAND architecture Flash memory devices as a synchronous memory device through an external synchronous memory interface; and buffering data access requests received through the external synchronous memory interface in a

buffer memory." As detailed above, Applicant submits that McClain fails to teach or disclose such a method. As such, McClain fails to teach or disclose all elements of independent claim 99.

Applicant respectfully contends that claims 1, 22, 27, 45, 60, 75, 94, 96, and 98-99 as pending have been shown to be patentably distinct from the cited reference of McClain. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(e) and allowance of claims 1, 22, 27, 45, 60, 75, 79, 94, 96 and 98-99.

Claim Rejections Under 35 U.S.C. § 103

Claims 2-4, 6-7, 23-26, 29-31, 47-49, 62, 65, 76, 78, 81 and 84 were rejected under 35 U.S.C. § 103(a) as being unpatentable over McClain in view of McCormack et al. (U.S. Patent No. 5,781,201). Applicant respectfully traverses this rejection and feels that claims 2-4, 6-7, 23-26, 29-31, 47-49, 62, 65, 76, 78, 81 and 84 are allowable for the following reasons.

Applicant respectfully continues to maintain, as stated above in regards to the rejection of independent claims 1, 22, 27, 45, 60, and 75, from which claims 2-4, 6-7, 23-26, 29-31, 47-49, 62, 65, 76, 78, 81 and 84 depend, that McClain only discloses a personal computer system 10 having a system control logic ASIC 68 coupled to several memory devices 16, 18, 20, and not a memory device itself. Applicant maintains that McClain does not teach or disclose that the system 10 presents itself, and the coupled memory devices 16, 18, 20, through an external SDRAM interface as being a SDRAM device in its own right or as emulating a SDRAM DRAM. Applicant therefore respectfully submits that McClain does not teach or disclose a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See*, McClain, Figures 1 and 2; Abstract; and Column 3, Line 20 to Column 5, Line 6.

In addition, Applicant respectfully continues to maintain that McCormack et al. discloses a method of read and write buffering to a video memory to allow for maximum bus utilization.

Applicant therefore respectfully submits that McCormack et al. does not disclose or suggest a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See, e.g.*, McCormack et al., Abstract.

Applicant thus respectfully submits that combining McClain with McCormack et al. does not teach or suggest the Applicant's claimed invention, as maintained by the Examiner. Applicant therefore respectfully contends that McClain and McCormack et al. do not teach or suggest all elements of Applicant's claims 1, 22, 27, 45, 60, and 75, either alone or in combination.

As such, Applicant respectfully contends that claims 1, 22, 27, 45, 60, and 75 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. As claims 2-4, 6-7, 23-26, 29-31, 47-49, 62, 65, 76, 78, 81 and 84 depend from and further define claims 1, 22, 27, 45, 60, and 75, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 2-4, 6-7, 23-26, 29-31, 47-49, 62, 65, 76, 78, 81 and 84.

Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over McClain in view of McCormack, further in view of Widdup (U.S. Patent No. 6,651,148). Applicant respectfully traverses this rejection and feels that claim 5is allowable for the following reasons.

Applicant respectfully continues to maintain, as stated above in regards to the rejection of independent claim 1, from which claim 5 depends, that McClain only discloses a personal computer system 10 having a system control logic ASIC 68 coupled to several memory devices 16, 18, 20, and not a memory device itself. Applicant maintains that McClain does not teach or disclose that the system 10 presents itself, and the coupled memory devices 16, 18, 20, through an external SDRAM interface as being a SDRAM device in its own right or as emulating a SDRAM DRAM. Applicant therefore respectfully submits that McClain does not teach or

disclose a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See*, McClain, Figures 1 and 2; Abstract; and Column 3, Line 20 to Column 5, Line 6.

In addition, Applicant respectfully continues to maintain that McCormack et al. discloses a method of read and write buffering to a video memory to allow for maximum bus utilization. *See, e.g.*, McCormack et al., Abstract.

Further, Applicant respectfully continues to maintain that Widdup discloses a memory controller that incorporates a read and write arbiter to allow pseudo-simultaneous memory transactions. Applicant therefore respectfully submits that Widdup does not disclose or suggest a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See, e.g.*, Widdup, Abstract; column 4, line 65 to column 5, line 11.

Applicant thus respectfully submits that combining McClain and McCormack et al. with Widdup does not teach or suggest the Applicant's claimed invention, as maintained by the Examiner. Applicant therefore respectfully contends that McClain, McCormack et al. and Widdup do not teach or suggest all elements of Applicant's claim 1, either alone or in combination.

As such, Applicant respectfully contends that claim 1 as pending has been shown to be patentably distinct from the cited references, either alone or in combination. As claim 5 depends from and further define claim 1, it is also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claim 5.

Claims 8, 32, 50, 63-64, 77 and 82-83 were rejected under 35 U.S.C. § 103(a) as being unpatentable over McClain in view of McCormack, further in view of Wallace et al. (U.S. Patent No. 6,628, 537). Applicant respectfully traverses this rejection and feels that claims 8, 32, 50, 63-64, 77 and 82-83 are allowable for the following reasons.

Applicant respectfully continues to maintain, as stated above in regards to the rejection of independent claims 1, 27, 45, 60, and 75, from which claims 8, 32, 50, 63-64, 77 and 82-83 depend, that McClain only discloses a personal computer system 10 having a system control logic ASIC 68 coupled to several memory devices 16, 18, 20, and not a memory device itself. Applicant maintains that McClain does not teach or disclose that the system 10 presents itself, and the coupled memory devices 16, 18, 20, through an external SDRAM interface as being a SDRAM device in its own right or as emulating a SDRAM DRAM. Applicant therefore respectfully submits that McClain does not teach or disclose a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See*, McClain, Figures 1 and 2; Abstract; and Column 3, Line 20 to Column 5, Line 6.

In addition, Applicant respectfully continues to maintain that McCormack et al. discloses a method of read and write buffering to a video memory to allow for maximum bus utilization. *See, e.g.*, McCormack et al., Abstract. Further, Applicant respectfully continues to maintain that Wallace et al. discloses a computer memory card that writes a BUSY signal into a status register and does not teach or disclose a READY/BUSY pin. Applicant therefore respectfully submits that Wallace et al. does not disclose or suggest a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a

synchronous memory device. *See, e.g.*, Wallace et al., Abstract; Figure 16, column 9, line 65 to column 10, line 40.

Applicant thus respectfully submits that combining McClain and McCormack et al. with Wallace et al. does not teach or suggest the Applicant's claimed invention, as maintained by the Examiner. Applicant therefore respectfully contends that McClain, McCormack et al. and Wallace et al. do not teach or suggest all elements of Applicant's claims 1, 27, 45, 60, and 75, either alone or in combination.

As such, Applicant respectfully contends that claims 1, 27, 45, 60, and 75 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. As claims 8, 32, 50, 63-64, 77 and 82-83 depend from and further define claims 1, 27, 45, 60, and 75, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 8, 32, 50, 63-64, 77 and 82-83.

Claims 9, 33, 51, 66 and 85 were rejected under 35 U.S.C. § 103(a) as being unpatentable over McClain in view Meyer (U.S. Patent No. 4,065,862). Applicant respectfully traverses this rejection and feels that claims 9, 33, 51, 66 and 85 are allowable for the following reasons.

Applicant respectfully continues to maintain, as stated above in regards to the rejection of independent claims 1, 27, 45, 60, and 75, from which claims 9, 33, 51, 66 and 85 depend, that McClain only discloses a personal computer system 10 having a system control logic ASIC 68 coupled to several memory devices 16, 18, 20, and not a memory device itself. Applicant maintains that McClain does not teach or disclose that the system 10 presents itself, and the coupled memory devices 16, 18, 20, through an external SDRAM interface as being a SDRAM device in its own right or as emulating a SDRAM DRAM. Applicant therefore respectfully submits that McClain does not teach or disclose a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a

synchronous memory device. *See*, McClain, Figures 1 and 2; Abstract; and Column 3, Line 20 to Column 5, Line 6.

In addition, Applicant respectfully continues to maintain that Meyer discloses an interface and method for synchronizing data signals and clock pulses across a data transmission system, such as a RS-232-C serial line, disclosing a "BUFFER FULL" signal line. Applicant maintains that Meyer does not disclose or suggest a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See, e.g.*, Meyer, Figures 1 and 2, Abstract; column 1, line 12 to column 4, line 25.

Applicant thus respectfully submits that combining McClain with Meyer does not teach or suggest the Applicant's claimed invention, as maintained by the Examiner. Applicant therefore respectfully contends that McClain and Meyer do not teach or suggest all elements of Applicant's claims 1, 27, 45, 60, and 75, either alone or in combination.

As such, Applicant respectfully contends that claims 1, 27, 45, 60, and 75 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. As claims 9, 33, 51, 66 and 85 depend from and further define claims 1, 27, 45, 60, and 75, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 9, 33, 51, 66 and 85.

Claims 14 and 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over McClain in view of Bartoli et al. (U.S. Patent No. 6,442,068). Applicant respectfully traverses this rejection and feels that claims 14 and 36 are allowable for the following reasons.

Applicant respectfully continues to maintain, as stated above in regards to the rejection of independent claims 1 and 27, from which claims 14 and 36 depend, that McClain only discloses a personal computer system 10 having a system control logic ASIC 68 coupled to several

memory devices 16, 18, 20, and not a memory device itself. Applicant maintains that McClain does not teach or disclose that the system 10 presents itself, and the coupled memory devices 16, 18, 20, through an external SDRAM interface as being a SDRAM device in its own right or as emulating a SDRAM DRAM. Applicant therefore respectfully submits that McClain does not teach or disclose a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See*, McClain, Figures 1 and 2; Abstract; and Column 3, Line 20 to Column 5, Line 6.

In addition, Applicant respectfully continues to maintain that Bartoli et al. discloses a non-volatile memory having the capability to suspend a programming or erase operation to conduct a burst or page mode read, and does not disclose or suggest a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See, e.g.*, Bartoli et al., Abstract; Summary.

Applicant thus respectfully submits that combining McClain with Bartoli et al. does not teach or suggest the Applicant's claimed invention, as maintained by the Examiner. Applicant therefore respectfully contends that McClain and Bartoli et al. do not teach or suggest all elements of Applicant's claims 1 and 27, either alone or in combination.

As such, Applicant respectfully contends that claims 1 and 27 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. As claims 14 and 36 depend from and further define claims 1 and 27, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 14 and 36.

Claims 15-16, 37-38, 69 and 88 were rejected under 35 U.S.C. § 103(a) as being unpatentable over McClain in view of the 'Background of Invention' (BOI) section of the present application. Applicant respectfully traverses this rejection and feels that claims 15-16, 37-38, 69 and 88 are allowable for the following reasons.

Applicant respectfully continues to maintain, as stated above in regards to the rejection of independent claims 1, 27, 60, and 75, from which claims 15-16, 37-38, 69 and 88 depend, that McClain only discloses a personal computer system 10 having a system control logic ASIC 68 coupled to several memory devices 16, 18, 20, and not a memory device itself. Applicant maintains that McClain does not teach or disclose that the system 10 presents itself, and the coupled memory devices 16, 18, 20, through an external SDRAM interface as being a SDRAM device in its own right or as emulating a SDRAM DRAM. Applicant therefore respectfully submits that McClain does not teach or disclose a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See*, McClain, Figures 1 and 2; Abstract; and Column 3, Line 20 to Column 5, Line 6.

In addition, Applicant respectfully continues to maintain that Paragraph [0005] of the BOI discloses only that to compensate for their higher error rates "and to take advantage of the inherent higher array density, NAND Flash memory typically utilizes error correction codes (ECC) and/or are interfaced to and presented as a mass storage device, such as a magnetic disk. In this manner the errors of a NAND Flash memory device can be addressed by the operating system/host/driver/firmware and/or the file system that the Flash device is formatted with." *See*, BOI of Present Application, Paragraph [0005]. As such, Applicant maintains that the BOI does not teach or suggest a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and

present them through the synchronous interface as a synchronous memory device. Furthermore, Applicant respectfully maintains that the BOI, while disclosing the use of ECC codes in NAND Flash memory devices, does not teach or suggest ECC hardware incorporated with the NAND Flash memory device or that SDRAM DRAM's utilize ECC codes. Applicant respectfully maintains that ECC codes are not utilized in volatile DRAM memory devices, ECC codes are known by those skilled in the art to be too slow and inappropriate for the access speed and size of the data generally stored in DRAM, and that one skilled in the art would therefore not utilize ECC codes with a memory device that presented itself as a read/write compatible SDRAM.

Applicant thus respectfully submits that combining McClain with the BOI does not teach or suggest the Applicant's claimed invention, as maintained by the Examiner. Applicant therefore respectfully contends that McClain and the BOI do not teach or suggest all elements of Applicant's claims 1, 27, 60, and 75, either alone or in combination.

As such, Applicant respectfully contends that claims 1, 27, 60, and 75 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. As claims 15-16, 37-38, 69 and 88 depend from and further define claims 1, 27, 60, and 75, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 15-16, 37-38, 69 and 88.

CONCLUSION

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. Please charge any further fees deemed necessary or credit any overpayment to Deposit Account No. 501373.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

Date: 4/5/07

Andrew C. Walseth
Reg. No. 43,234

Attorneys for Applicant
Leffert Jay & Polglaze
P.O. Box 581009
Minneapolis, MN 55458-1009
T 612 312-2200
F 612 312-2250